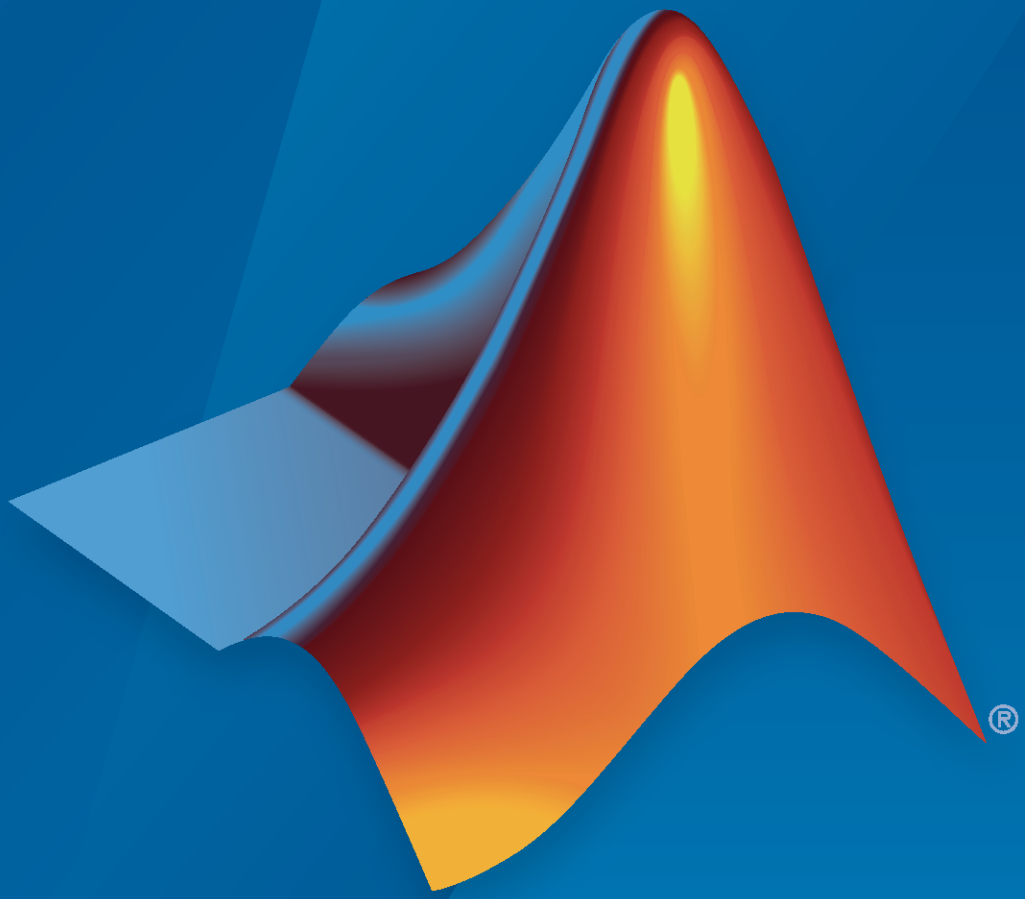
Mixed-Signal Blockset™ Release Notes



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The MathWorks, Inc.
1 Apple Hill Drive
Natick, MA 01760-2098

Mixed-Signal Blockset™ Release Notes

Contents

R2022a

R2021b

R2021a

R2020b

R2020a

R2019b

R2019a

R2022a

Version: 2.2

New Features

Bug Fixes

Updated Lowpass Resampler: Generate output sample times

The Lowpass Resampler block now allows you to generate output sample times if you need them.

Clock Generator and Signal Sampler: Model clock recovery

Use the Clock Generator to generate clock signal with one or multiple phases. Use the Signal Sampler to sample the incoming signal at the edge of an incoming clock. Together, they can help model clock recovery loops.

Improved Mixed-Signal Analyzer app: Import Cadence data faster

You can now import the Cadence® simulation data faster into the **Mixed Signal Analyzer** app.

R2021b

Version: 2.1

New Features

Bug Fixes

Operational Amplifier: Model double pole or multiple pole operational amplifier

Use the Operational Amplifier block to model an operational amplifier. You can design a double pole operational amplifier from circuit parameters or a multiple pole operational amplifier from a transfer function.

Delta Sigma Modulator: Model delta sigma modulator ADC

Use the Delta Sigma Modulator block to model a delta sigma modulator ADC. You can design a feedback or feed-forward modulator with a cascade of integrators or resonators to model ADCs of orders 2 to 6.

R2021a

Version: 2.0

New Features

Bug Fixes

Mixed-Signal Analyzer App: Analyze and visualize mixed-signal simulation data, trends, and waveforms

Introducing the **Mixed Signal Analyzer** app to analyze and visualize generic mixed-signal simulation data. This app also provides access to the Cadence Virtuoso® Analog Design Environment (ADE) using the Cadence Virtuoso ADE — MATLAB Integration option.

Ring Oscillator VCO: Parameterize physical model of oscillator phase noise

Use ring-oscillator-based VCO for PLL applications tailored to your specifications. Ring Oscillator VCO comes with negligible initialization time, efficient execution, and most importantly, it models the well understood oscillator phase noise behavior.

Jitter Calculation in Clock Signals: Introducing Clock Jitter Measurement block

Measure RMS period jitter, cycle-to-cycle (C2C) jitter, and duty cycle distortion (DCD) in periodic signals using the Clock Jitter Measurement block.

Precision Analog Conversion of Large Digital Words: Introducing Segmented DAC block

Use the Segmented DAC block to convert large digital words into analog signals.

Continuous-Time Analysis of Discrete-Time Outputs: Introducing Lowpass Resampler block and lowpassResample function

Use the Lowpass Resampler block to enable blocks with discrete-time outputs support continuous-time analyses in Simulink®.

Use the `lowpassResample` function to perform the same computations in the MATLAB® environment.

Additional Performance Metrics in Data Converters: Measure noise floor, settling time, and distortions

Measure the noise floor and settling time of DACs. You can also measure the total harmonic distortion (THD) and intermodulation distortion (IMD) characterized by the third-order intercept in ADCs. For more information, see ADC Measurement and Testbenches and DAC Measurement and Testbenches.

Binary Vector Conversion: Introducing Binary Vector Conversion block

Convert scaler integer values to binary coded logical vector and vice versa using the Binary Vector Conversion block. You can also resize a logical vector and reverse the bit-index arrangement of the vector.

R2020b

Version: 1.3

New Features

Create or Modify Linear Circuits: Introducing Linear Circuit Wizard block

Use the Linear Circuit Wizard block to create a new linear circuit or modify an existing one. Import the linear circuit from a SPICE netlist, modify the input and output ports, and define various device noises of interest.

Simulation Performance: Run simulations faster by using Accelerator mode in Simulink

Mixed-Signal Blockset blocks now support the Accelerator mode in Simulink. For information about this mode, see How Acceleration Modes Work (Simulink).

Measure Basic Timing Metrics: Introducing Timing Measurement block

Use the Timing Measurement block to measure basic timing metrics such as period, frequency, rise time, fall time, duty cycle, and delay.

Phase Noise Measurement Algorithm: Improved phase noise measurement using zero-crossing threshold

The Phase Noise Measurement block now uses an updated algorithm using zero-crossing times. This algorithm provides improved phase noise measurement without oversampling. You can also plot the phase noise profile any time during the simulation.

Phase Noise and Jitter Measurement: phaseNoiseMeasure function updated and phaseNoiseToJitter function added

Use the updated `phaseNoiseMeasure` function to measure phase noise either from power spectrum or from time domain data. Introducing the `phaseNoiseToJitter` function to measure RMS phase jitter in seconds, radians, or degrees.

Timing Metrics Measurement: Introducing timeDomainSignal2RiseTime, timeDomainSignal2FallTime, and timeDomainSignal2DutyCycle functions

Use the `timeDomainSignal2RiseTime`, `timeDomainSignal2FallTime`, and `timeDomainSignal2DutyCycle` functions to measure the rise time, fall time, and duty cycle of a time domain signal.

R2020a

Version: 1.2

New Features

Bug Fixes

Digital to Analog Converter: Introducing Binary Weighted DAC and relevant measurement and testbench blocks

Use the Binary Weighted DAC block as a starting point to model digital to analog converters. Also use DAC AC measurement, DAC DC measurement, and DAC Testbench blocks to validate the Binary Weighted DAC, or a DAC of your own implementation.

Nonlinearity Measurement in Data Converters: Introducing function inldnl

Using the `inldnl` function, you can measure the differential and integral nonlinearities of ADCs and DACs.

Phase Noise Measurement in PLL: Introducing function phaseNoiseMeasure

Using the `phaseNoiseMeasure` function, you can measure and plot phase noise profile at specific frequency offset points.

R2019b

Version: 1.1

New Features

Bug Fixes

New ADC Examples: Learn how to evaluate the performance of different ADCs

Explore new featured examples to learn how to design and evaluate different types of ADCs such as successive approximation ADC, interleaved ADC, and subranging ADC. You can analyze ADCs with impairments and measure their offset error, gain error, and linearity.

R2019a

Version: 1.0

New Features

Introducing Mixed-Signal Blockset: Design, simulate, and verify analog and mixed-signal systems

Mixed-Signal Blockset provides models of components and impairments, analysis tools, and test benches for designing and verifying mixed-signal integrated circuits (ICs).

You can model PLLs, data converters, and other systems at different levels of abstraction and explore a range of IC architectures. You can customize models to include impairments such as noise, nonlinearity, and quantization effects, and refine the system description using a top-down methodology.

Using the test benches provided, you can verify system performance and improve modeling fidelity by fitting measurement characteristics or circuit-level simulation results. Rapid system-level simulation using variable-step Mixed-Signal Blockset solvers lets you debug the implementation and identify design flaws before simulating the IC at the transistor level.

With Mixed-Signal Blockset you can simulate mixed-signal components together with complex DSP algorithms and control logic. As a result, both analog and digital design teams can work from the same executable specification.

White-Box Behavioral Models of PLL and ADC: Design and analyze mixed-signal systems based on typical architectures using data-sheet specifications

Use the provided PLL models such as Fractional N PLL with Analog Compensation, Fractional N PLL with Delta Sigma Modulator, Integer N PLL with Dual Modulus Prescaler, Integer N PLL with Single Modulus Prescaler to design and simulate your own customized PLL at the system level. Verify and visualize the open loop and closed loop responses.

Use the provided ADC architectures Flash ADC and SAR ADC to design and simulate your own customized ADC at the system level.

White-Box Building Blocks: Design custom mixed-signal systems following a top-down methodology

Mixed-Signal Blockset provides white-box building blocks that you can use to design custom mixed-signal systems. See the PLL Building Blocks and ADC Building Blocks for more information.

Models of Impairments: Model timing effects, phase noise, jitter, leakage, and other impairments

Model rise/fall times, finite slew rate, and variable time delays in your feedback loop for both PLL and ADC systems.

Model the phase noise in PLL system. For more information, see Phase Noise at PLL Output.

Model the aperture jitter, offset error, and gain error in ADCs.

Measurement Blocks and Testbenches: Verify the performance of PLL and ADC with application-specific metrics

Use the provided Measurements and Testbenches to

- Measure the lock time, phase noise profile, operating frequency of a PLL.
- Characterize the performance of building blocks such as VCO, PFD, and charge pump.
- Measure AC and DC characteristics and aperture jitter of ADCs.

Mixed-Signal Blockset Models: Explore an add-on library with additional mixed-signal models for ADCs, PLLs, SerDes, and SMPS (Introduced April 2019)

Mixed-Signal Blockset provides an add-on library called Mixed-Signal Blockset Models that contains additional mixed-signal system models for ADCs, PLLs, SerDes, and SMPS.

To access the Mixed-Signal Blockset Models, first download the Mixed-Signal Blockset Models from the Add-On Explorer.